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1	BRS	L1	1985	(circuit adj design) and verification	USPAT	2004/05/20 10:27
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3	BRS	L3	31	(circuit adj design) and (verification.ti.) and reduction	USPAT	2004/05/20 10:30
4	BRS	L4	6	(circuit adj design) and verification and (gate near reduction)	USPAT	2004/05/20 10:31
5	BRS	L5	16	(circuit adj design) and verification and (circuit near reduction)	USPAT	2004/05/20 10:33
6	BRS	L6	6	(circuit adj design) and (design near verification) and (circuit near reduction)	USPAT	2004/05/20 10:39
7	BRS	L7	0	(circuit adj design) and (correction near probes)	USPAT	2004/05/20 10:39
8	BRS	L8	274	(circuit adj design) and (correction and probes)	USPAT	2004/05/20 10:39
9	BRS	L9	0	(circuit adj design) and (correction adj probes)	USPAT	2004/05/20 10:39
10	BRS	L10	42	circuit and (correction adj probes)	USPAT	2004/05/20 10:52
11	BRS	L11	0	cone adj binary adj decision	USPAT	2004/05/20 10:53
12	BRS	L12	0	cone adj binary adj decision	USPAT	2004/05/20 11:12
13	BRS	L13	894	binary adj decision	USPAT	2004/05/20 11:12
14	BRS	L14	21	(binary adj decision) and verification and (digital adj design)	USPAT	2004/05/20 11:21
15	BRS	L20	12	(binary adj decision) and verification and (digital adj design) and debugging	USPAT	2004/05/20 11:22
16	BRS	L21	2	(binary adj decision) and verification and (digital adj design) and debugging and reduction	USPAT	2004/05/20 11:27

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1	BRS	L1	158	717/155-156.ccls.	USPAT	2004/05/20 14:14
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4	BRS	L4	0	717/155-156.ccls. and optimize and EDA and BDD	USPAT; US-PG PUB	2004/05/20 14:15
5	BRS	L5	18	EDA and BDD	USPAT; US-PG PUB	2004/05/20 14:15
6	BRS	L6	18	EDA and BDD	USPAT; US-PG PUB; IBM_T DB	2004/05/20 15:04
7	BRS	L7	55	ashar.in.	USPAT; US-PG PUB; IBM_T DB	2004/05/20 15:04